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***mentalSPICE™ V2.0***  
**for Windows 95/98/NT/ME/2000/XP**

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# 1 Introduction

SPICE analog circuit simulators allow you to develop and checkout a circuit design before you actually build it. SPICE stands for Simulation Program with Integrated Circuit Emphasis and traces its origins to the University of California at Berkeley. With the schematic editor, SuperCAD, you can draw up a circuit schematic and click over **Analog Simulation...** in the UTILITIES menu and thereby run the SPICE simulation. After the simulation, SuperCAD reloads the schematic, and you can then probe various signals using the scope popout display. The whole process is easy and completely automatic, and it is done entirely within the SuperCAD environment. You are free to treat your design as though it were implemented on a virtual breadboard, which you can test using virtual instruments (such as the oscilloscope display). You can easily alter portions of the circuit or make corrections and then re-run the simulation to see the effects. Using a 386 or greater machine with a hard disk, the process of changing the circuit and seeing the result can be measured in seconds for a small to medium sized circuit.

**mentalSPICE** is Mental Automation's version of Berkeley SPICE, version 3F5.

**mentalSPICE** is great at checking out circuits such as the following:

- Filters
- Oscillators
- Amplifiers
- Power circuits
- Transmission lines

You can simulate anything that is made up out of passive components (resistors, inductors, or capacitors) or active discretes (transistors, diodes, etc.). You can also simulate circuits that include ICs that have models. The models are generally available from IC manufacturers such as National, TI, and Motorola; in addition **mentalSPICE** comes with models for common opamp s.

The latest version of **mentalSPICE** now includes models for basic digital circuits so that you can also do limited digital simulation as well as mixed mode (both analog and digital) simulation. If you have need for a lot of digital simulation capability, the **SuperSIM** digital simulator is available as an add-on to SuperCAD.

## 1.1 System Requirements

mentalSPICE will operate on IBM compatible computers meeting the following requirements:

Memory	1M or greater
Graphics	Any display with MS Windows 3.x driver
Printers	Any printer with MS Windows 3.x driver
Mouse	Microsoft (serial or bus) compatible (use <u>required</u> )
Disk drive	Hard drive with 2MB or greater space
Software	Windows 95/98/ME/NT/2000 or greater, SuperCAD™ schematic editor

Note also that mentalSPICE requires a math coprocessor. If you have a 486DX or Pentium™ machine, the coprocessor is already provided.

## 1.2 Installation

**Note:** Be sure to install SuperCAD before installing mentalSPICE.

You can use the INSTALL program to install mentalSPICE on a hard disk. To use it, place the distribution disk in floppy drive A or B and then click on RUN in the FILE menu of the Windows Program Manager. Enter "A:INSTALL" or "B:INSTALL" in the Command Line box, and then click on the OK button. The install program will first ask for a drive letter (e.g., "c" or "d") and a name for the subdirectory (e.g., "supercad") that you wish to use for mentalSPICE. After this,

the program copies all files to your hard drive. During the installation, SPICE examples are copied to the EXAMPLES subdirectory of SuperCAD and special SPICE symbols are copied to the library directory.

### ***1.3 Organization of Manual***

General operation of mentalSPICE in the SuperCAD/Windows environment is described in Chapter 2. The general organization of a SPICE netlist, which is the input to mentalSPICE, is presented in chapter 3. Chapters 4 and 5 describe the built-in SPICE models and the basic analysis types respectively. Note that much of the material in Chapters 3-5 is based on the SPICE 3 Version 3F5 User's Manual.

### ***1.4 References for SPICE***

SPICE is widely used in many businesses, schools, and universities, and there are many good references for it. Here is a list of four of these:

- 1) Rashid, Muhammad H., **Spice for Circuits and Electronics Using PSPICE®**, Second Edition, Prentice Hall, 1995
- 2) Vladimirescu, Andrei, **The SPICE Book**, John Wiley & Sons, Inc., 1994
- 3) Rashid, Muhammad H., **SPICE for Power Electronics and Electric Power**, Prentice Hall, 1993
- 4) Tuinenga, Paul W., **SPICE: A guide to Circuit Simulation & Analysis Using PSPICE®**, Prentice Hall, 1995, 1992, 1988

### ***1.5 Technical Support***

For technical support call or write Mental Automation at:

6603 84<sup>th</sup> Street CT NW  
Gig Harbor WA 98332  
(253) 858-8104  
FAX: (253) 858-8105  
Internet:<http://www.mentala.com>

You can also email schematic files with questions to us at [mentala@mentala.com](mailto:mentala@mentala.com). If you send schematics make sure that all unique library part files are also provided.

## ***2 Operation and Examples***

### ***2.1 Preparation of Schematic for Simulation***

SPICE simulation using SuperCAD works best with small to medium-complexity analog circuits that can fit on a single sheet. You can work with multiple sheets but you may have to switch from one sheet to another to view different signals. The steps for preparing a schematic for simulation are as follows:

a) Draw the schematic----be sure you use parts that correspond to the SPICE built-in parts (transistors, diodes, etc.) or those in SPICE libraries.

b) Give all parts component values by using the VALUE operation in the AUX menu. If you don't have enough room for a value, use the append statement, as in the following example:

```
#&V1 SIN 0 3.1 500KHZ
```

c) Label circuit nodes with number labels (1,2,3,...). Any node with the ground symbol on it becomes part of node 0 when the netlister is run. If you do not number a node, the SuperCAD netlister will automatically number it, starting with index 100.

d) Provide a circuit input stimulus---For transient simply place the FUNGEN (function generator) symbol on the schematic and wire it to the input point. Double click over the part to set it up with the appropriate signal waveform (sine, pulse, piece-wise linear, or FM) For AC analysis, place the SWEEPGEN (sweep generator) part on the schematic and wire it to the circuit input. For DC analysis, use the voltage source symbol (VOLTS).

e) Mark all signals to be probed (traced) in the simulation by using the MARK operation in the DISPLAY pulldown menu. You first have to click over MARK and then click over any signal that is to be probed (you can remove a signal by clicking so that the asterisk disappears).

f) If you need to measure current in a branch, insert the AMMETER symbol there. If you run a transient analysis, the current waveform will be automatically displayed (signal name: Vn#, where n is the reference number of the symbol).

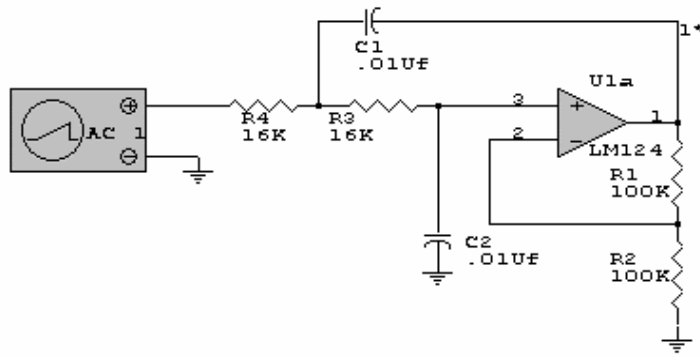
g) Add any SPICE special commands (such as the .IC command or .MODEL command) to the schematic using the text operation; these commands should be preceded by the # character.

The current version of SuperCAD and the netlister only allow one kind of primary analysis at a time, which is selected using the mentalSPICE setup menu:

- a) .TRAN (timing analysis)
- b) .AC (AC frequency analysis)
- c) .DC (DC characteristics analysis)

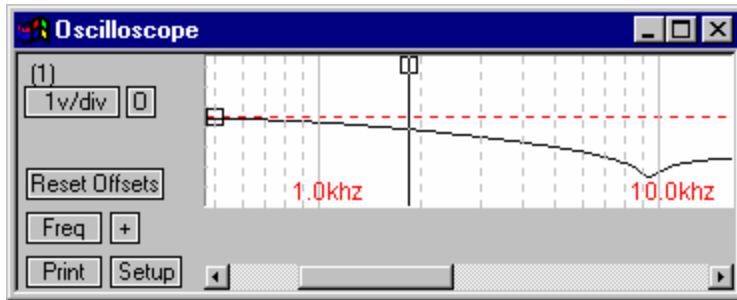
You can also select the static .OP analysis independently. You can easily change the analysis type by changing the information in the setup menu and doing some changes with the signal generators in your schematic.

The following shows an example of a SPICE simulation schematic (low-pass filter, using an LM124):



This example is set up for frequency analysis (as indicated by the presence of the input sweep generator). +5-volt power is supplied to the opamp through use of the power supply symbol. Note that the model for the opamp resides in the ANALOG.MOD file.

The resulting frequency plot on the oscilloscope display is as follows:



## 2.2 Referencing and Using External IC Library Models

mentalSPICE comes with models for many standard library parts. These include parts in the Analog library, Harris Semiconductor parts, Generic (74xxx) parts, and CMOS parts. To use these models you simply place the corresponding symbol on the schematic. All of the models reside in .MOD files, whose root name is the same as the corresponding symbol sub-directory. For example, the LM324 model is in the ANALOG.MOD file, since the LM324.PIC symbol file is in the ANALOG subdirectory of the SuperCAD library. Parts whose symbols are located in the SuperCAD LIB sub-directory are put in the SPICE.MOD file.

Appendix A lists currently available IC parts. See the on-line mentalSPICE help manual for parts added since this manual was produced.

You can also add new custom or vendor-supplied Integrated Circuit (IC) Models. To do this, you simply put the given model information in one of the .MOD files, located in the SuperCAD library sub-directory. If necessary you can create a new .MOD file---just use the name of an existing library part sub-directory where the SuperCAD symbol exists. You can use NOTEPAD or a similar ASCII editor to append a new model file into the given .MOD file.

Usually vendor supplied models do not reflect the actual pinout of IC packages; so some work is needed to map the model pinout to real-world packages. Most models from National Semiconductor, for instance, use a 5-pin standard pinout To convert one of these, a header is added to the model such as in the following:

```
.SUBCKT LM258 1 2 4 5 6 7 8
XA 3 2 8 4 1 LM258X
XB 5 6 8 4 7 LM258X
.
.
.SUBCKT LM258X          1    2    99    50    28
[body of model]
```

```
.ENDS LM258X
.ENDS
```

The LM258X referenced is the original vendor model. You also have to add an extra .ENDS statement to the end of the model.

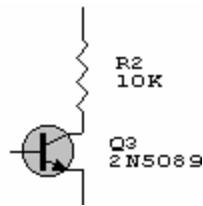
Note that SPICE requires all IC designators to be “X” type. To accommodate this, the SuperCAD netlister automatically prefaces all the IC “U” type designators with an “X”. For example U12 becomes XU12.

Note that some massaging of vendor-supplied models may be necessary to make them compatible with a SPICE3 simulator such as mentalSPICE. The primary massaging is automatic---the translation of the SPICE2 “poly” statements in many of the models is accomplished in the netlister. The translation currently handles all poly(1) and poly(2) cases and the low order poly(n) cases where n>2.

### 2.3 Referencing and Using External Semiconductor Models

You can make use of custom or vendor-supplied semiconductor models. To do this you simply put the given model information in the SEMICON.MOD file, located in the SuperCAD sub-directory. You can use NOTEPAD or a similar ASCII editor to append a new model file.

To reference a model, give the semiconductor symbol on your schematic a value whose name is the model name. For example, in the following



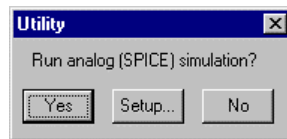
the value 2N5089” refers to the model statement in SEMICON.MOD as listed below:

```
.model 2N5089 NPN(Is=5.911f Xti=3 Eg=1.11 Vaf=62.37 Bf=1.434K Ne=1.421
+ Ise=5.911f Ikf=15.4m Xtb=1.5 Br=1.262 Nc=2 Isc=0 Ikr=0 Rc=1.61
+ Cjc=4.017p Mjc=.3174 Vjc=.75 Fc=.5 Cje=4.973p Mje=.4146 Vje=.75
+ Tr=4.671n Tf=822.3p Itf=.35 Vtf=4 Xtf=7 Rb=10)
```

Semiconductor models for any diode or transistor can be placed in the SEMICON.MOD file.

### 2.4 Running and Viewing the Simulation Results

Once the schematic is prepared as discussed above, you can run the simulation by clicking over **Analog Simulation...** in the UTILITIES menu , and a dialog box will appear, as follows:



To establish the type of simulation and other items, click on the SETUP button.

Once you start the operation, the current schematic is saved, SuperCAD is temporarily suspended, and the netlister is run. The netlister produces a SPICE netlist file with the name of the current schematic as the root name and the extension .CIR. This is read by mentalSPICE and the simulation proceeds. After a delay that depends on the complexity of the

simulation, SuperCAD becomes active again. You can now view the latest simulation results by clicking over the DISPLAY menu and then clicking over the SCOPE function. This brings up the oscilloscope display window. Signals that are marked in the schematic are automatically loaded and displayed. You can move the window over the circuit, so that it doesn't obscure the signals of interest, by dragging over the title bar. To change the display of a specific signal, click over one of the four trace labels and then click over any marked signal on the schematic. Marked signals are indicated by a "\*" suffix. Up to 200 samples per channel are loaded from the trace buffer file on disk when a given signal is accessed.

Note that the maximum viewable signal level is 327 in absolute magnitude (32768/100). Also the minimum detectable signal change that the oscilloscope can see is 10 millivolts; this is at the .1 volts/div setting. This range of display should be satisfactory for most cases, but if it is not, you can generally adjust the level of signal sources to accommodate it.

To read signal amplitudes in both display channels at a given point, the readout cursor is used; this is the vertical line in the scope display. To read a value, simply drag the line left or right with the mouse. When the left mouse button is released, the signal values are printed on the dialog line. For DC and TRAN analysis, the units are in volts. For AC analysis the units are decibels or degrees.

The "m" key is used to select loading of either phase values or magnitudes from the .OUT file; both values are generated automatically when you do an AC analysis.

Gain values for each channel are automatically selected based on the peak signal level of signals loaded from the .OUT file. The units used (volts, decibels, and degrees/div) are likewise read from the file.

## ***2.5 Troubleshooting***

Sometimes mentalSPICE may fail to produce an output file. The first indication of this is the message:

Can't find signal X in buffer

where X is the signal name (usually the node number). This message occurs when you try to display the output with the oscilloscope. If this happens, look in the file **ERROR.DOC** for more information; this file will be in the same subdirectory as your SPICE schematic. You should also look in the .OUT file, if one is produced.

Depending on the nature of the problem noted in the files, there are several things you should do:

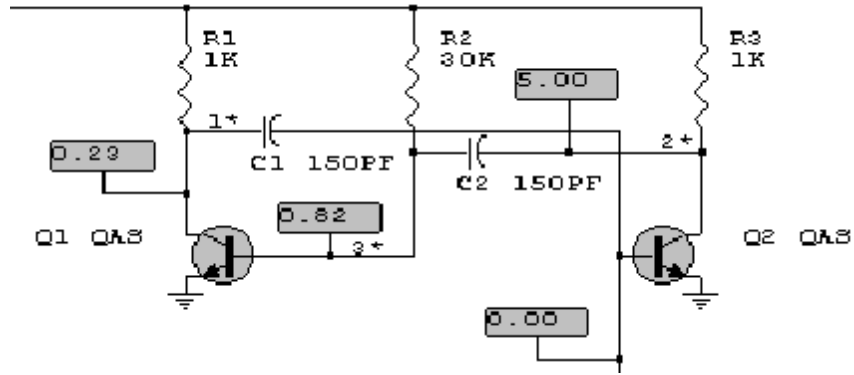
- ? Check the schematic for obvious problems, such as missing connections & components
- ? Check for correct component values
- ? Check for correct units

If a node number is noted in the messages in the file, this is a good place to look on the schematic.

Sometimes SPICE fails to reach a solution, even when everything looks OK on the schematic. Convergence is a known problem under some circumstances---see one of the books referenced in Section 1.4. Another cause for failure is lack of good initial conditions for the circuit--this is especially true in circuits like oscillators. You can use the .IC statement to initialize nodes to a known value, or (if you have capacitors), use the IC parameter in the value field.

## ***2.6 Virtual Voltmeters and Ammeters***

You can measure the DC voltages at various points in a circuit by doing an Operating Point Analysis (.OP) and by connecting the voltmeter part (VMETER) to those points. After running the SPICE analysis, the meters are updated with the voltage values, as in the following example:



To measure AC current through a branch you can insert the AMMETER symbol:



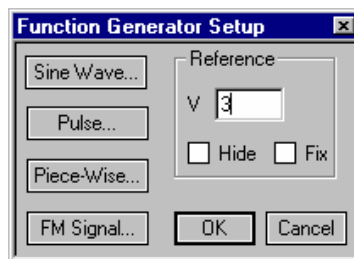
In this example, the current signal name (as seen in the SPICE output file and in the oscilloscope signal label) is V3#”.

## 2.7 Virtual Signal Generators and Power Sources

mentalSPICE uses special signal and power source library parts. These are shown below. To use the parts, access them by clicking on the library button and placing them on the schematic; wire the terminals to the appropriate places.

### Function Generator (FUNGEN)

This part can be used to specify various time waveforms, including sinusoidal, piecewise linear, pulse, and frequency modulated signals. To select one of the signal types just double click over the part. This will bring up the following dialog:



Click on the appropriate button to select a signal type. This will bring up a setup dialog, as well as select one of the four possible symbols:

sine wave



piece-wise linear



pulse



FM



### **AC Sweep Generator**

This part is used as the signal source in the frequency (AC) analysis of a circuit



### **DC Power Supply**

This part is used to specify a DC power source. To specify the power voltage level, double-click on the part and enter the voltage as the value.

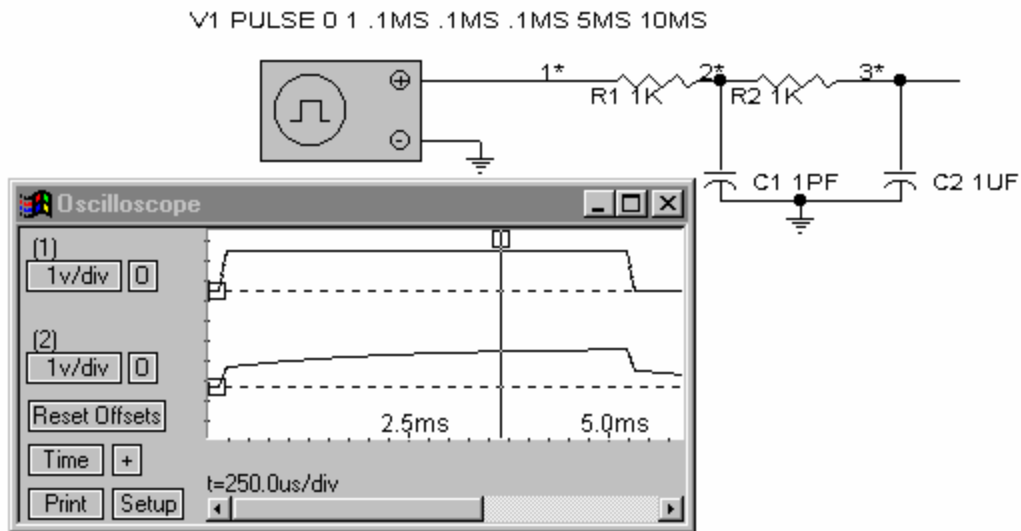


## ***2.8 Examples***

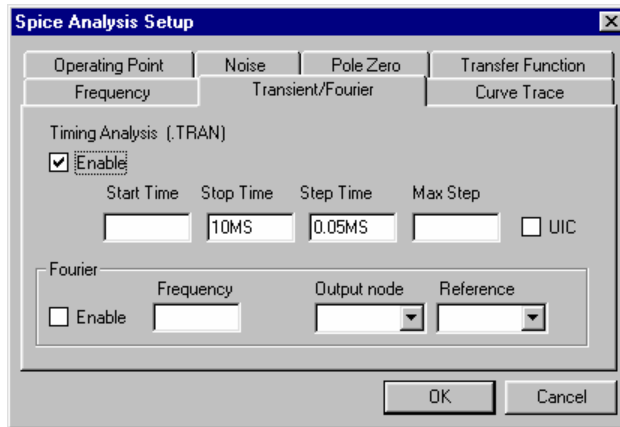
The examples discussed in this section can all be found in the EXAMPLES subdirectory on the SPICE examples disk.

### ***2.8.1 RC Circuit***

The figure below shows the first example, which is a simple RC circuit. This circuit only requires two control statements. The pulse generator (one of the four possible function generator options) specifies an input waveform in the form of a 5MS pulse lasting the 10MS



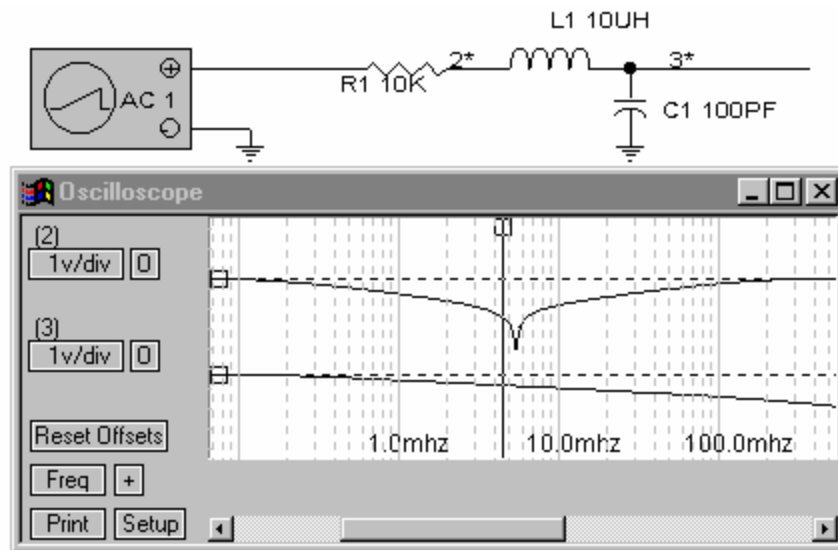
The circuit is setup for a timing analysis as follows:



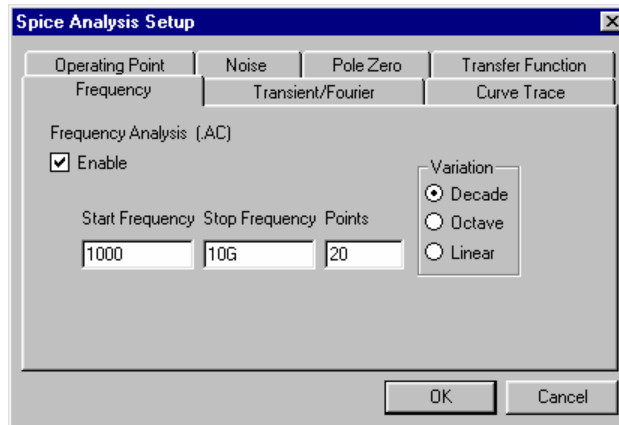
This tells the SPICE simulator to do a timing analysis for a duration of 10MS in .05MS steps, which yields 200 samples; the start time is 0. Note that the software will automatically check the step time and adjust it so that 200 samples are produced in any case.

## 2.8.2 RLC Circuit

The second example shown below is a circuit for which we do a frequency analysis. The circuit input is connected to the sweep generator (SWEEPGEN part).



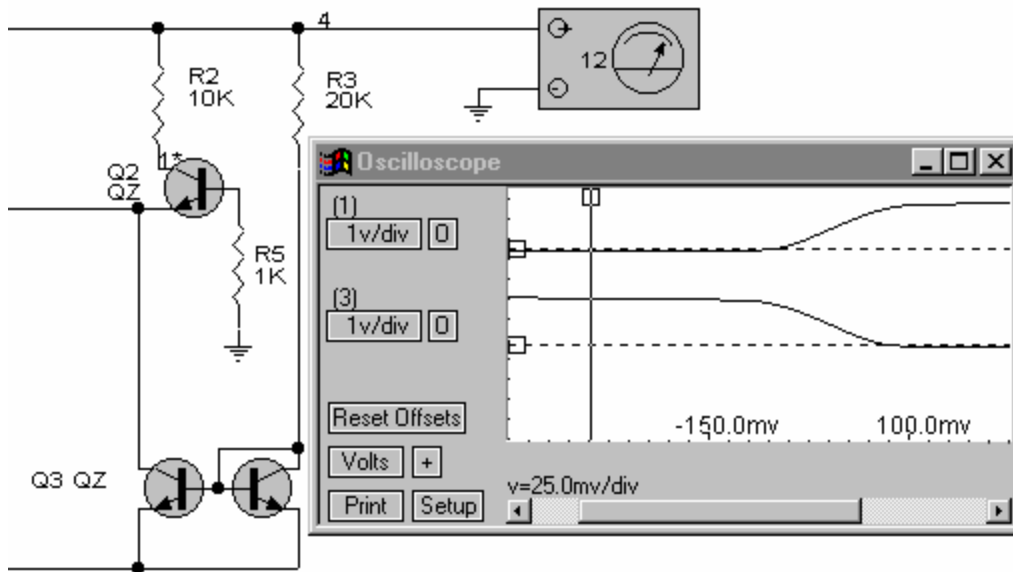
This analysis is setup for a frequency analysis as follows:



Every decade of frequency (factor of 10 increase), 40 samples are collected, and we select 10 decades of analysis, 1Hz to 10Ghz, giving 200 samples. In this example, the output is automatically measured in decibel units. The "volts" units in the display should be read as decibels in this case.

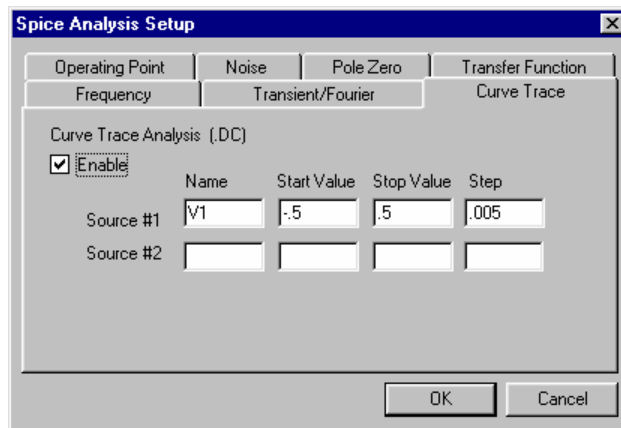
### 2.8.3 Differential Pair

The figure below shows the example of a differential pair circuit.



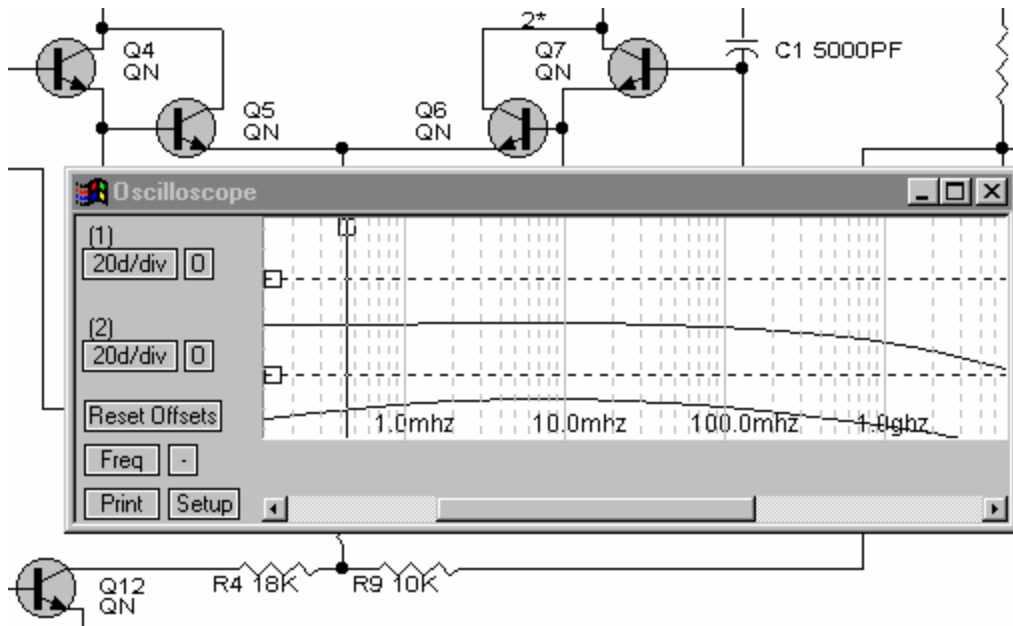
In this case we are measuring various node voltages as a function of the input voltage that is applied to node 5. Parameters for the transistor are provided within the .MODEL statement. Note that this statement is all in one line (but it almost uses the whole line). If necessary, you can use multiple lines to specify a control statement; but make sure that the successive lines are entered immediately after the first line, using the "+" character. You can also place this model in the SEMICON.LIB file and achieve the same result as placing it on the schematic.

The setup for this example is as follows:



### 2.8.4 UA709 Operational Amplifier

A partial view of the UA709 amplifier and a frequency plot is shown in below. As in the case of the RLC circuit above, the units in the display should be read as decibels (d). In this example there are two power supplies.



The setup for the circuit is also the same as the RLC circuit and it specifies an AC analysis from 1 to 10GHZ with a DECADE variation.

### 2.8.5 Op Amp Differentiator Circuit

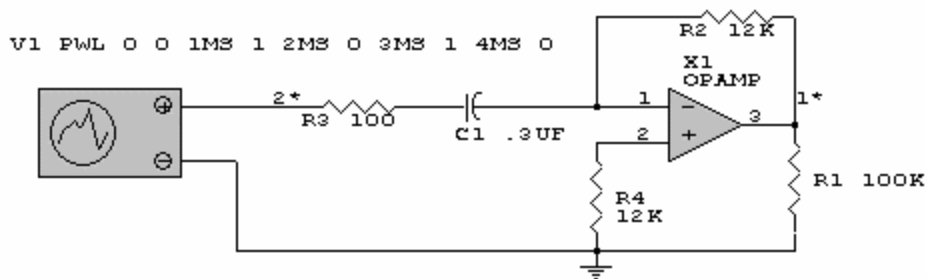
This circuit illustrates the use of an idealized op amp circuit. The op amp is modeled using the following subcircuit statements:

```

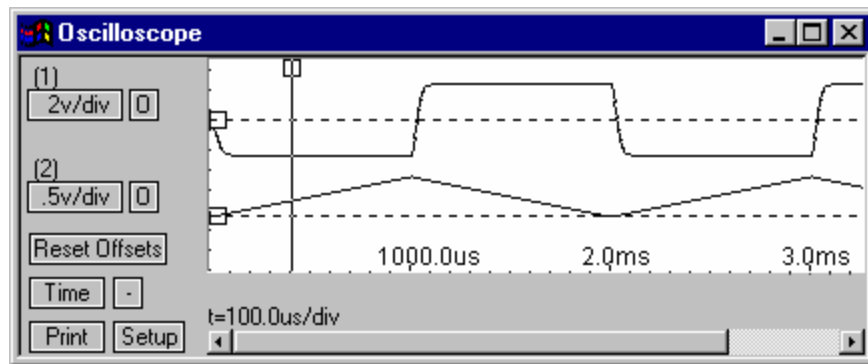
* Model for OPAMP
.SUBCKT OPAMP 1 2 6
RI 1 2 2.0E6
*voltage controlled source
G1 0 3 1 2 0.1M
R1 3 0 10K
C1 3 0 1.5UF
*voltage controlled voltage source
E1 0 5 3 0 2E+5
RO 5 6 75
.ENDS

```

In this example, these statements are placed in the SPICE.MOD file, since the opamp symbol comes from the SPICE symbol library (SPICE.CON). The complete schematic for a differentiator circuit is shown below:

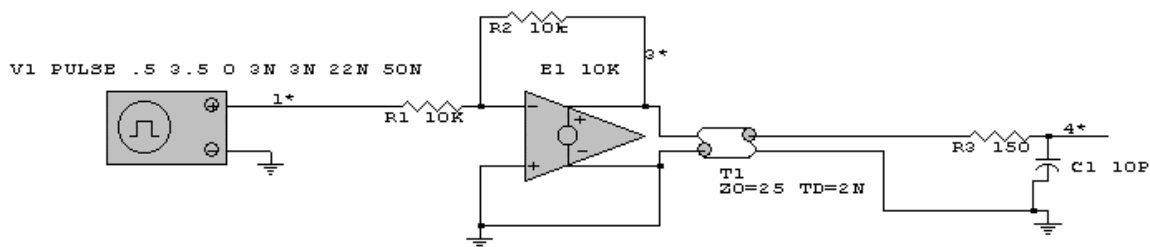


The PWL function assigns a sawtooth waveform to the voltage generator V. The resulting waveforms after the SPICE simulation are shown as follows:

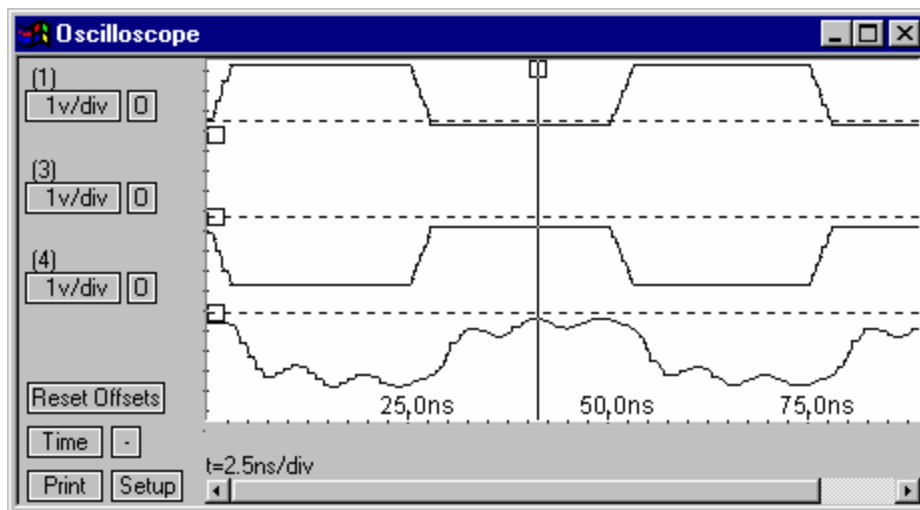


## 2.8.6 Transmission Line

This example uses the ideal transmission line model. The circuit is as follows:

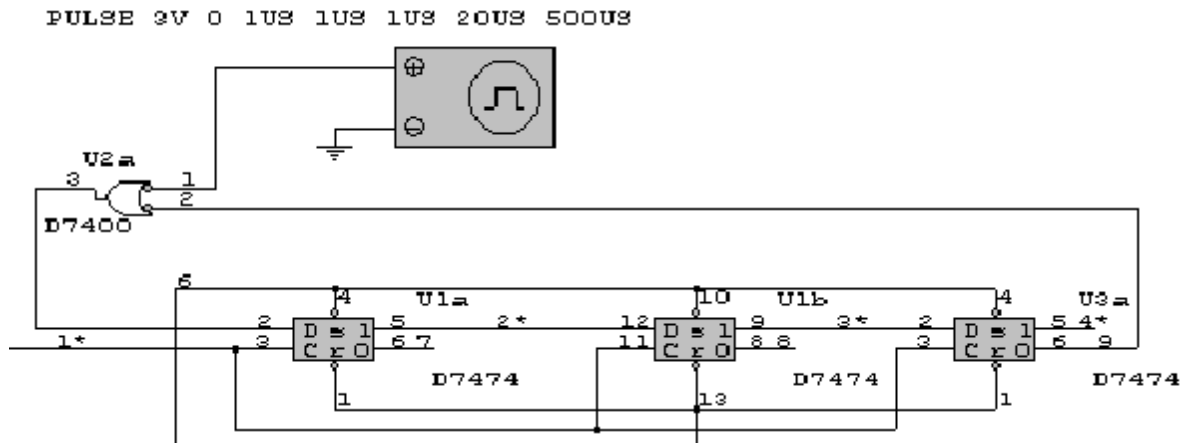


The symbol for the transmission line is TRANSMIS, which corresponds to the 4-terminal SPICE transmission line model (see section 4.11). The resulting waveforms are as follows:

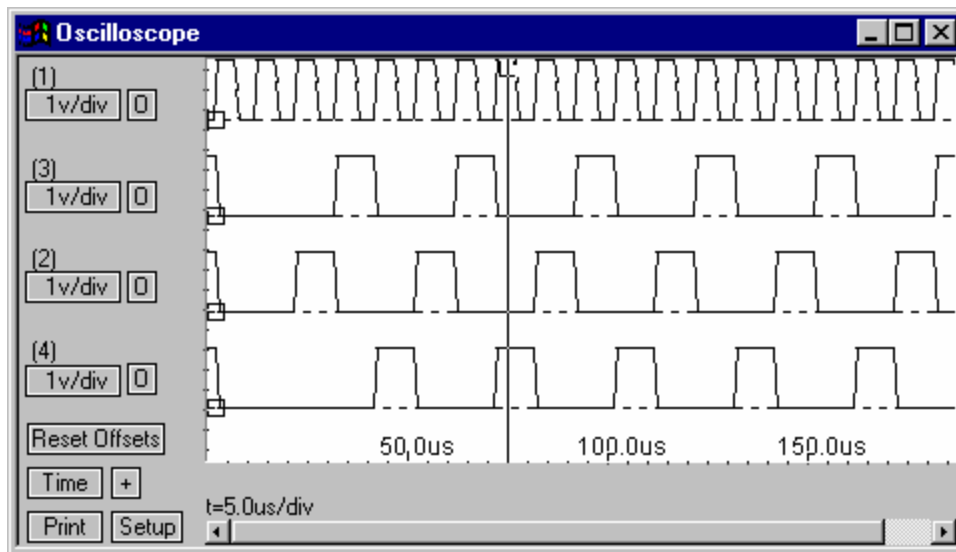


## 2.8.7 Digital Circuit Example

This example shows the use of a 7400 gate and a 7474 TTL flip-flop to make a 3-bit circular shift register. Note that the symbols for the TTL parts are just standard SuperCAD 74xxx symbols. A transient analysis is performed from 0 to 200mS, with a .5mS step.

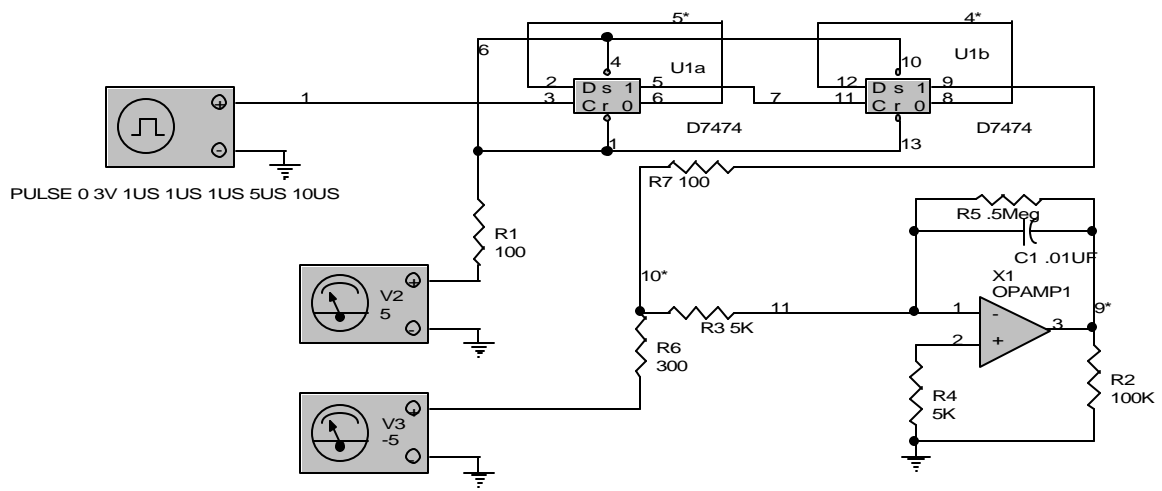


The resulting waveforms are shown as follows:

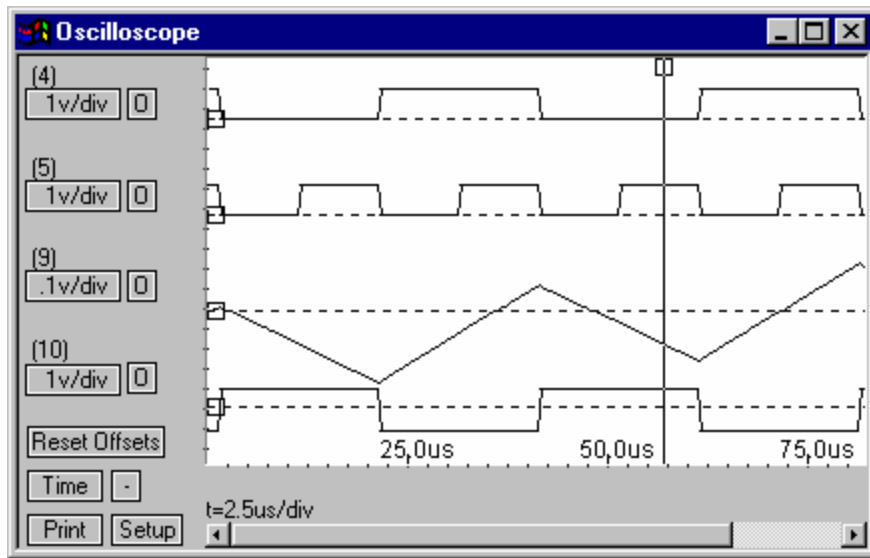


### 2.8.8 Mixed mode Simulation Example

In this example a digital divide-by-4 circuit is combined with an opamp integrator circuit to produce a sawtooth waveform:



The models for the D-type flip-flops (D7474s) are specified in GENERIC.MOD. The waveforms are as follows:



### 3 SPICE Netlist Description

mentalSPICE accepts text (ASCII) files which have an extension .CKT. The netlist files are produced automatically from the SuperCAD schematic editor when you load a schematic and click on **Analog Simulation...** in the **Utilities** menu. Note that the netlist files can be edited and viewed by any ASCII editor such as Notepad.

#### 3.1 General Netlist Structure and Conventions

The general format of a SPICE netlist is as follows:

```
Title  
[netlist body]  
.END
```

For example:

```
*SPICE NET  
R1 1 2 1K  
C1 2 0 1PF  
R2 2 3 1K  
C2 3 0 1UF  
.TRAN 50US 10MS  
VIN 1 0 PULSE 0 1 .1MS .1MS .1MS 5MS 10MS  
.PRINT TRAN V(1) V(2) V(3)  
.END
```

The netlist body describes the circuit layout and includes model parameters and SPICE analysis controls. The order of the lines in the netlist body is arbitrary, except where continuation lines are used. A line may be continued by entering a '+' (plus) in the first column of the following line.

Each component in the circuit is specified by a netlist line that contains the component name, the circuit nodes to which the component is connected, and the values of the parameters that determine the electrical characteristics of the component. The first letter of the component name specifies the component type. The format for the SPICE component types is provided below. The strings *name1*, *name2*, and *name3* in the formats represent arbitrary alphanumeric strings of up to 7 characters.

Fields on a line are separated by one or more blanks, a comma, an equal (=) sign, or parentheses. Added spaces are ignored.

A name field must begin with a letter (A through Z) and can contain only letter and number characters.

A number field may be an integer field, a floating point field, either an integer or floating point number followed by an integer exponent (for example, 2e-12 or 1.23e3), or either an integer or a floating point number followed by one of the following scale factors:

```
T=1012  
G = 109  
Meg = 106  
K=103  
Mil = 25.4-6  
M=10-3  
U = 10-6  
N = 10-9  
P=10-12  
F = 10-15
```

Letters immediately following a number that are not scale factors are ignored, and letters immediately following a scale factor are ignored.

Nodes names in mentalSPICE must be a number, e.g. 1, 2, 3. The ground node must be named "0" (zero). The SuperCAD netlister will automatically provide node number names (starting at 100), if a node is unnamed in the schematic. Also, nodes which are attached to the ground symbol (GND) are automatically placed on node "0".

## 3.2 Device Models

Netlist statement:

```
.MODEL MODNAME TYPE(PNAME1=PVAL1 PNAME2=PVAL2 ...)
```

Examples:

```
.MODEL MOD1 NPN (BF=50 IS=1e-13 VBF=50)
```

Simple circuit components typically require only a few parameter values. However, some devices (especially, semiconductor devices) require many parameter values. In a given circuit, many devices may be defined by the same set of device model parameters. In this case it is convenient to define a set of device model parameters in a separate MODEL line with a unique model name. The devices can then refer to the model name.

MODNAME in the above is the model name, and TYPE is one of the following types:

D	Diode model
NPN	NPN BJT model
PNP	PNP BJT model
NJF	N-channel JFET model
PJF	P-channel JFET model
NMOS	N-channel MOSFET model
PMOS	P-channel MOSFET model

Parameter values are defined by appending the parameter name followed by an equal sign and the parameter value. Model parameters that are not given a value are assigned the default values given below for each model type. Models, model parameters, and default values are listed in the next section along with the description of device component lines.

## 3.3 Subcircuits

A subcircuit that consists of SPICE elements can be defined and referenced in a fashion similar to device models. The subcircuit is defined in the input file by a grouping of component lines; the program then automatically inserts the group of elements wherever the subcircuit is referenced. There is no limit on the size or complexity of subcircuits, and subcircuits may contain other subcircuits.

### 3.3.1 SUBCKT Line

Netlist statement:

```
.SUBCKT subnam N1 [N2 N3 ... ]
```

Examples:

```
.SUBCKT OPAMP 1 2 3 4
```

A circuit definition is begun with a .SUBCKT line. SUBNAM is the subcircuit name, and N1, N2,... are the external nodes, which cannot be zero. The group of component lines that immediately follow the .SUBCKT line define the subcircuit. The last line in a subcircuit definition is the ENDS line (see below). Control lines may not appear within a subcircuit

definition; however, subcircuit definitions may contain anything else, including other subcircuit definitions, device models, and subcircuit calls (see below). Note that any device models or subcircuit definitions included as part of a subcircuit definition are strictly local (i.e., such models and definitions are not known outside the subcircuit definition). Also, any component nodes not included on the SUBCKT line are strictly local, with the exception of 0 (ground), which is always global.

### ***3.3.2 ENDS Line***

Netlist statement:

```
.ENDS [SUBNAM]
```

Examples:

```
.ENDS OPAMP
```

The "Ends" line is the last line in a subcircuit definition. The subcircuit name, if included, indicates which subcircuit definition is being terminated; if omitted, all subcircuits being defined are terminated. The name is needed only when nested subcircuit definitions are being made.

### ***3.3.3 Subcircuit Calls***

Netlist statement:

```
Xname2 N1 [N2 N3 ... ] SUBNAM
```

Examples:

```
XI 2 4 17 3 1 MULTI
```

Subcircuits are used in SPICE by specifying pseudo-elements beginning with the letter X, followed by the circuit nodes to be used in expanding the subcircuit

## ***4 SPICE Circuit Elements and Models***

Fields that are enclosed in brackets ("[ ]") are optional. With respect to branch currents and voltages, SPICE always assumes that current flows in the direction of voltage drop.

### ***4.1 Resistors***

Netlist statement:

```
Rname1 N1 N2 VALUE
```

Examples:

```
R1 1 2 51  
ROUT 16 19 20K
```

N1 and N2 are the two resistor nodes. VALUE is the resistance in ohms and may be positive or negative but not zero.

### ***4.2 Capacitors***

Netlist statement:

**Cname1** N+ N- VALUE [IC=INCOND]

Examples:

```
C12 5 0 25PF
CIN 17 23 10U IC=4V
```

N+ and N- are the positive and negative capacitor nodes, respectively. VALUE is the capacitance in Farads. The initial condition is the initial value of capacitor voltage in volts. The initial conditions apply only if the UIC option is specified on the TRAN control line.

### **4.3 Inductors**

Netlist statement:

**Lname2** N+ N- VALUE [IC=INCOND]

Examples:

```
L3 5 6 1UH
LFILTER 10 17 20U IC=6.9MA
```

N+ and N- are the positive and negative inductor nodes, respectively. VALUE is the inductance in Henries. The initial condition is the initial value of inductor current in amps that flows from N+, through the inductor, to N-. The initial conditions apply only if the UIC option is specified on the TRAN analysis line.

### **4.4 Mutual Inductors**

Netlist statement:

**Kname1 Lname2 Lname3** VALUE

Examples:

```
K1 L1 L2 0.98
KTRANS L1 L2 0.791
```

**Lname2** and **Lname3** are the names of the two coupled inductors, and VALUE is the coefficient of coupling, K, which must be greater than 0 and less than or equal to 1.

### **4.5 Independent Sources**

Netlist statement(s):

**Vname1** N+ N- [[DC] DC/TRAN VALUE] [AC [ACMAG [ACPHASE]]]

**Iname2** N+ N- [[DC] DC/TRAN VALUE] [AC [ACMAG [ACPHASE]]]

Examples:

```
V1 10 0 DC 6
V2 24 2 0.002 AC 1 SIN(0 1 1MEG)
I3 23 21 AC 0.345 45.0 SFFM(0 1 10K 5 1K)
VAMMETER 30 31
```

N+ and N- are the positive and negative nodes, respectively. Voltage sources need not be grounded. Positive current is assumed to flow from the positive node, through the source, to the negative node. A positive current source forces current to flow out of the N+ node, through the source, and into the N- node. Voltage sources, in addition to being used for circuit excitation, are the "ammeters" for SPICE: zero valued voltage sources may be inserted into the circuit in order to measure current. When used this way they have no effect on circuit operation because they represent short-circuits. Note that the special SPICE symbol, AMMETER, is a voltage source, which can be used for this purpose.

DC/TRAN is the dc and transient analysis value of the source. If the source value is zero both for dc and transient analyses, this value may be omitted. If the source value is time-invariant (for example, in a power supply), then the value may be preceded by the letters DC.

ACMAG is the ac magnitude and ACPHASE is the ac phase. The source is set to this value in the ac analysis. If ACMAG is omitted following the keyword AC, a value of unity is assumed. If ACPHASE is omitted, a value of zero is assumed. If the source is not an ac small-signal input, the keyword AC and the ac values are omitted.

Any independent source can be assigned a time-dependent value for transient analysis. If a source is assigned a time-dependent value, the time-zero value is used for dc analysis. There are five independent source functions: pulse, exponential, sinusoidal, piece-wise linear, and single-frequency FM. If parameters other than source values are omitted or set to zero, the default values shown are assumed. (TSTEP is the printing increment and TSTOP is the final time (see the TRAN control line for explanation)).

### 4.5.1 Pulse

Netlist statement:

PULSE(V1 V2 TD TR TF PW PER)

Examples:

V1 3 0 PULSE(0 5 5NS 5NS 5NS 100NS 500NS)

<u>parameter</u>	<u>default value</u>	<u>units</u>
V1 (initial value)		Volts or Amps
V2 (pulsed value)		Volts or Amps
TD (delay time)	0.0	seconds
TR (rise time)	TSTEP	seconds
TF (fall time)	TSTEP	seconds
PW (pulse width)	TSTOP	seconds
PER(period)	TSTOP	seconds

A single pulse so specified is described by the following table:

<u>time</u>	<u>value</u>
0	V1
TD	V1
TD+TR	V2
TD+TR+PW	V2
TD+TR+PW+TF	V1
TSTOP	V1

Intermediate points are determined by linear interpolation.

### 4.5.2 Sinusoidal

Netlist statement:

SIN(VO VA FREQ TD THETA)

Examples:

VIN 3 0 SIN(0 5.5 10MEG 10NS IEIO)

<u>parameters</u>	<u>default value</u>	<u>units</u>
VO (offset)		Volts or Amps
VA (amplitude)		Volts or Amps
FREQ (frequency)	1/TSTOP	Hz
TD (delay)	0.0	seconds
THETA (damping factor)	0.0	1/seconds

The shape of the waveform is described by the following table:

<u>time</u>	<u>value</u>
0 to TD	VO
TD to TSTOP	$VO + VA e^{-(t - TD)THETA} \sin(2 \text{ FREQ}(t + TD))$

### 4.5.3 Exponential

Netlist statement:

EXP(V1 V2 TD1 TAU1 TD2 TAU2)

Examples:

V5 12 0 EXP(0 -3 20NS 50NS 200NS 100NS)

<u>parameter</u>	<u>default value</u>	<u>units</u>
V1 (initial value)		Volts or Amps
V2 (pulsed value)		Volts or Amps
TD1 (rise delay time)	0.0	seconds
TAU1 (rise time constant)	TSTEP	seconds
TD2 (fall delay time)	TD1+TSTEP	seconds
TAU2 (fall time constant)	TSTEP	seconds

The shape of the waveform is described by the following table:

<u>time</u>	<u>value</u>
0 to TD1	V1
TD1 to TD2	$V1 + (V2 - V1)[1 - e^{-(t - TD1)/TAU1}]$
TD2 to TSTOP	$V1 + (V2 - V1)[1 - e^{-(t - TD1)/TAU1}] + (V1 - V2)[1 - e^{-(t - TD2)/TAU2}]$

### 4.5.4 Piece-Wise Linear

Netlist statement:

PWL(T1 V1 [T2 V2 T3 V3 T4 V4 ... ])

Examples:

V2 1 2 PWL(0 0 5 20NS 5 40NS 0 50NS)

Each pair of values (Ti, Vi) specifies that the value of the source is Vi (in Volts) at time=Ti. The value of the source at intermediate time points is determined by using linear interpolation. The PWL statement can also be used for current sources. In this case, pairs (Ti, Ii) specify the values, where Ii is in Amps.

### 4.5.5 Single-Frequency FM

Netlist statement:

SFFM(VO VA FC MDI FS)

Examples:

VI 12 0 SFFM(0 1 1MEG 2 20K)

<u>parameter</u>	<u>default value</u>	<u>units</u>
VO (offset)	0.0	Volts or Amps
VA (amplitude)	0.0	Volts or Amps
FC (carrier frequency)	1/TSTOP	Hz
MDI (modulation index)	0.0	-
FS (signal frequency)	1/TSTOP	Hz

The shape of the waveform is described by the following:

$$V(t)=VO+ VA \sin(2 \text{ FC } t + MDI \sin(2 \text{ FS } t))$$

### 4.6 Linear Voltage-Controlled Current Sources

Netlist statement:

**Gname1** N+ N- NC+ NC- VALUE

Example:

G14 0 5 0 1E-3

N+ and N- are the positive and negative nodes, respectively. Current flow is from the positive node, through the source, to the negative node. NC+ and NC- are the positive and negative controlling nodes, respectively. VALUE is the transconductance (in mhos).

### 4.7 Linear Voltage-Controlled Voltage Sources

Netlist statement:

**Ename1** N+ N- NC+ NC- VALUE

Example:

E1 5 3 7 1 2.0

N+ is the positive node, and N- is the negative node. NC+ and NC- are the positive and negative controlling nodes, respectively. VALUE is the voltage gain.

## 4.8 Linear Current-Controlled Current Sources

Netlist statement:

**Fname**I N+ N- VNAME VALUE

Example:

F1 5 6 V13 5

N+ and N- are the positive and negative nodes, respectively. Current flow is from the positive node, through the source, to the negative node. VNAME is the name of a voltage source through which the controlling current flows. The direction of positive controlling current flow is from the positive node, through the source, to the negative node of VNAME. VALUE is the current gain.

## 4.9 Linear Current-Controlled Voltage Sources

Netlist statement:

**Hname**I N+ N- VNAME VALUE

Example:

H3 8 23 V11 2.5K

N+ and N- are the positive and negative nodes, respectively. VNAME is the name of a voltage source through which the controlling current flows. The direction of positive controlling current flow is from the positive node, through the source, to the negative node of VNAME. VALUE is the transresistance (in ohms).

## 4.10 Non-linear Dependent Sources

Netlist statement:

**Bname**I N+ N- [I=EXPR] [V=EXPR]

Examples:

B1 0 1 I=sin(v(3))  
B2 3 4 I=17  
B3 0 12 V=exp(pi\*i(v(4,5)))

N+ is the positive node, and N- is the negative node. The values of the V and I parameters determine the voltages and currents across and through the device, respectively. If I is given, the device is a current source. If V is given, the device is a voltage source. Only one of these parameters can be used at a time.

The variable EXPR is an arbitrary function of the node voltages and currents in the circuit and can be a combination of the following elementary functions:

abs acos acosh asin asinh atan atanh cos cosh exp ln log sin sinh sqrt tan

## 4.11 Transmission Lines

Netlist statement:

**Tname**I N1 N2 N3 N4 ZO=VALUE [TD=VALUE] [F=FREQ [NL=NRMLEN]] + [IC=V1, I1, V2, I2]

Examples:

```
TI 1 0 2 0 ZO=62 TD=15NS
```

N1 and N2 are the nodes at port 1; N3 and N4 are the nodes at port 2. ZO is the characteristic impedance. The length of the line may be expressed in either of two forms:

- 1) The transmission delay, TD, may be specified directly (as TD=10ns, for example).
- 2) A frequency F may be given, together with NL, the normalized electrical length of the transmission line with respect to the wavelength in the line at the frequency F. If a frequency is specified but NL is omitted, 0.25 is assumed (i.e., the frequency is assumed to be the quarter-wave frequency).

Note that although both forms for expressing the line length are indicated as optional, one of the two must be specified.

This component models only one propagating mode. If all four nodes are distinct in the actual circuit, then two modes may be excited. To simulate such a situation, two transmission-line elements are required.

The initial condition specification consists of the voltage and current at each of the transmission line ports. Initial conditions apply only if the UIC option is specified on the TRAN control line.

## ***4.12 Semiconductors***

### ***4.12.1 Junction Diodes***

Netlist statement:

```
Dname1 N+ N- MODNAME [AREA] [OFF] [IC=VD] [TEMP=T]
```

Examples:

```
D2 2 10 DIODE1  
DCLMP 3 7 DMOD 3.0 IC=0.67
```

N+ is the positive node (anode), and N- is the negative nodes (cathode). MODNAME is the model name, AREA is the area factor, and OFF indicates a starting condition on the device for dc analysis. If the area factor is omitted, a value of 1.0 is assumed. The initial condition specification using IC=VD is intended for use with the UIC option on the TRAN control line, when a transient analysis is desired starting from other than the quiescent operating point. The TEMP value is the temperature at which this device operates, and overrides the temperature specification on the OPTION control line.

### ***4.12.2 Diode Model***

The dc characteristics of the diode are determined by the parameters IS and N. RS is the diode resistance. Charge storage effects are modeled by a transit time, TT, and a nonlinear depletion layer capacitance, which is determined by the parameters CJO, VJ, and M. The temperature dependence of the saturation current is defined by the parameters EG, the energy and XTI, the saturation current temperature exponent. The nominal temperature at which these parameters were measured is TNOM, which defaults to the circuit-wide value specified on the OPTIONS control line. Reverse breakdown is modeled by an exponential increase in the reverse diode current and is determined by the parameters BV and IBV; both of these are positive numbers. (\* = scales with area)

See the **mentalSPICE** on-line help file for further description of these parameters.

### ***4.12.3 Bipolar Junction Transistors (BJTs)***

Netlist statement:

```
Qname1 NC NB NE [NS] MODNAME [AREA] [OFF] [IC=VBE, VCE] [TEMP=T]
```

Examples:

```
Q23 10 24 13 QMOD IC=0.6, 5 .0  
Q50A 11 26 4 20 MOD1
```

NC, NB, and NE are the collector, base, and emitter nodes, respectively. NS is the substrate node. If unspecified, ground is used. MODNAME is the model name, AREA is the area factor, and OFF indicates an initial condition on the device for the dc analysis. If the area factor is omitted, a value of 1.0 is assumed. The initial condition specification using IC=VBE, VCE is intended for use with the UIC option on the TRAN control line, when a transient analysis is desired starting from other than the quiescent operating point. See the IC control line description for a better way to set transient initial conditions. The TEMP value is the temperature at which this device is to operate. and overrides the temperature specification on the OPTION control line.

#### ***4.12.4 BJT Models (NPN/PNP)***

The bipolar junction transistor model in SPICE is based on the integral charge control model of Gummel and Poon. The model automatically simplifies to the simpler Ebers-Moll model when certain parameters are not specified.

The dc model is defined by the parameters IS, BF, NF, ISE, IKF, and NE which determine the forward current gain characteristics, IS, BR, NR, ISC, IKR, and NC which determine the reverse current gain characteristics, and VAF and VAR which determine the output conductance for forward and reverse regions. Three ohmic resistances RB, RC, and RE are included, where RB can be high current dependent. Base charge storage is modeled by forward and reverse transit times, TF and TR, the forward transit time TF being bias dependent if desired, and nonlinear depletion layer capacitances which are determined by CJE, VJE, and MJE for the B-E junction, CJC, VJC, and MJC for the B-C junction and CJS, VJS, and MJS for the C-S (Collector-Substrate) junction. The temperature dependence of the saturation current, IS, is determined by the energy-gap, EG, and the saturation current temperature exponent, XTI. Additionally base current temperature dependence is modeled by the beta temperature exponent XTB in the new model. The values specified are assumed to have been measured at the temperature TNOM, which can be specified on the OPTIONS control line or overridden by a specification on the MODEL line.

See the **mentalsPICE** on-line help file for further description of these parameters.

#### ***4.12.5. Junction Field-Effect Transistors (JFETS)***

Netlist statement:

```
Jname1 ND NG NS MODNAME [AREA] [OFF] [IC=VDS, VGS] [TEMP=T]
```

Examples:

```
J2 7 2 3 JMI OFF
```

ND, NG, and NS are the drain, gate, and source nodes, respectively. MODNAME is the model name, AREA is the area factor, and OFF indicates an initial condition on the device for de analysis. If the area factor is omitted, a value of 1.0 is assumed. The initial condition specification, using IC=VDS, VGS is intended for use with the UIC option on the TRAN control line, when a transient analysis is desired starting from other than the quiescent operating point. See the IC control line for a better way to set initial conditions. The TEMP value is the temperature at which this device is to operate, and overrides the temperature specification on the OPTION control line.

#### ***4.12.6 JFET Models (NJF/PJF)***

The JFET model is derived from the FET model of Shichman and Hodges. The dc characteristics are defined by the parameters VTO, BETA, LAMBDA and IS. VTO and BETA determine the variation of drain current with gate voltage. LAMBDA determines the output conductance. IS specifies the saturation current of the two gate junctions. Two ohmic resistances, RD and RS, are included. Charge storage is modeled by nonlinear depletion layer capacitances for both gate junctions which vary as the -1/2 power of junction voltage and are defined by the parameters CGS, CGD, and PB.

See the **mentalSPICE** on-line help file for further description of these parameters.

### 4.12.7 MOSFETs

Netlist statement:

```
MnameI ND NG NS NB MODNAME [L=VAL] [W=VAL] [AD=VAL] [AS=VAL] + [PD=VAL] [PS=VAL] [NRD=VAL]
[NRS=VAL] [OFF] + [IC=VDS, VGS, VBS] [TEMP=T]
```

Examples:

```
MI 24 2 0 20 TYPE1
M31 2 17 6 10 MODM L=5U W=2U
MI 2 9 3 0 MOD1 L=10U W=5U AD=100P AS=100P PD=40U PS=40U
```

ND, NG, NS, and NB are the drain, gate, source, and bulk (substrate) nodes, respectively. MODNAME is the model name. L and W are the channel length and width, in meters. AD and AS are the areas of the drain and source diffusions, in meters<sup>2</sup>. Note that the suffix U specifies microns (1e-6 m) and P sq-microns (1e12 m<sup>2</sup>). If any of L, W, AD, or AS are not specified, default values are used. The use of defaults simplifies input file preparation, as well as the editing required if device geometries are to be changed. PD and PS are the perimeters of the drain and source junctions, in meters. NRD and NRS designate the equivalent number of squares of the drain and source diffusions; these values multiply the sheet resistance RSH specified on the MODEL control line for an accurate representation of the parasitic series drain and source resistance of each transistor. PD and PS default to 0.0 while NRD and NRS to 1.0. OFF indicates an (optional) initial condition on the device for de analysis. The (optional) initial condition specification using IC=VDS, VGS, VBS is intended for use with the UIC option on the TRAN control line, when a transient analysis is desired starting from other than the quiescent operating point. See the IC control line for a better and more convenient way to specify transient initial conditions. The (optional) TEMP value is the temperature at which this device is to operate, and overrides the temperature specification on the OPTION control line.

### 4.12.8 MOSFET Models (NMOS/PMOS)

mentalSPICE provides several MOSFET device models, which differ in the formulation of the I-V characteristic. The variable LEVEL specifies the model to be used:

LEVEL--1	Shichman-Hodges
LEVEL--2	MOS2
LEVEL--3	MOS3

The dc characteristics of the level 1 through level 3 MOSFETs are defined by the device parameters VTO, KP, LAMBDA, PHI and GAMMA. These parameters are computed by SPICE if process parameters (NSUB, TOX, ...) are given, but user-specified values always override. VTO is positive (negative) for enhancement mode and negative (positive) for depletion mode N-channel (P-channel) devices. Charge storage is modeled by three constant capacitors, CGSO, CGDO, and CGBO which represent overlap capacitances, by the nonlinear thin-oxide capacitance which is distributed among the gate, source, drain, and bulk regions, and by the nonlinear depletion-layer capacitances for both substrate junctions divided into bottom and periphery, which vary as the MJ and MJSW power of junction voltage respectively, and are determined by the parameters CBD, CBS, CJ, CJSW, MJ, MJSW and PB. Charge storage effects are modeled by the piecewise linear voltages-dependent capacitance model proposed by Meyer. The thin oxide charge-storage effects are treated slightly different for the LEVEL=1 model. These voltage dependent capacitances are included only if TOX is specified in the input description and they are represented using Meyer's formulation.

There is some overlap among the parameters describing the junctions, e.g. the reverse current can be input either as IS (in A) or as JS (in A/M2). Whereas the first is an absolute value the second is multiplied by AD and AS to give the reverse current of the drain and source junctions respectively. This methodology has been chosen since there is no sense in relating always junction characteristics with AD and AS entered on the device line; the areas can be defaulted. The same idea applies also to the zero-bias junction capacitances CBD and CBS (in F) on one hand, and CJ (in F/m2) on the other. The parasitic drain and source series resistance can be expressed as either RD and RS (in ohms) or RSH (in ohms/sq.), the latter being multiplied by the number of squares NRD and NRS input on the device line.

See the **mentalsPICE** on-line help file for further description of these parameters.

## ***5 Analysis and Support Commands***

The following command lines select analyses, set initial conditions, or specify output plots.

### ***5.1 Simulator Variables (.Options)***

The options line allows the user set options for specific simulation purposes.

Netlist statement:

```
.OPTIONS OPT1 OPT2...      (or OPT=OPTVAL ...)
```

Examples:

```
.OPTIONS TEMP=40 RELTOL=.003
```

See the **mentalsPICE** on-line help file for a description of the options.

### ***5.2 Initial Conditions***

#### ***5.2.1 .NODESET: Set Initial Node Voltage***

Netlist statement:

```
.NODESET V(N)=VALUE V(N)=VALUE
```

Examples:

```
.NODESET V(3)=13.23 V(5)=1.23
```

The .NODESET line helps the program find the dc or initial transient solution by making a preliminary pass with the indicated nodes held to the given voltages. The restriction is then released and the iteration continues to the true solution. The NODESET line may be necessary for convergence on bistable or astable circuits. In general, this line only needs to be used in special circumstances.

#### ***5.2.2 .IC: Set Initial Conditions***

Netlist statement:

```
.IC V(N)=VALUE V(N)=VALUE ...
```

Examples:

```
.IC V(1)=3 V(2)=-5.2
```

The IC line sets transient initial conditions. There are two interpretations of it as follows:

1) When the UIC parameter is specified on the TRAN line, then the node voltages specified on the IC control line are used to compute the capacitor, diode, BJT, and MOSFET initial conditions. This is equivalent to specifying the IC=... parameter on each device line, but is more convenient. The IC=... parameter can still be specified and takes precedence over the IC values. Since no dc bias (initial transient) solution is computed before the transient analysis, one should take care to specify all dc source voltages on the IC control line if they are to be used to compute device initial conditions.

2) When the UIC parameter is not specified on the TRAN control line, the dc bias (initial transient) solution is computed before the transient analysis. In this case, the node voltages specified on the IC control line is forced to the desired initial values during the bias solution. During transient analysis, the constraint on these node voltages is removed. This is the preferred method, since it allows SPICE to compute a consistent dc solution.

The IC line should not be confused with the NODESET line. The NODESET line is used to aid dc convergence, and does not affect the final solution, except for multi-stable circuits.

## 5.3 Analyses

### 5.3.1 .AC: Small-Signal AC Analysis

The AC analysis of SPICE determines the small signal frequency response of a circuit. The analysis is performed from a starting frequency value to a final value.

Netlist statements:

```
.AC DEC ND FSTART FSTOP  
.AC OCT NO FSTART FSTOP  
.AC LIN NP FSTART FSTOP
```

Examples:

```
.AC DEC 10 1K 10MEG  
.AC LIN 50 1 200HZ
```

DEC represents decade variation, and ND is the number of points per decade. OCT represents octave variation, and NO is the number of points per octave. LIN represents linear variation, and NP is the number of points. FSTART is the starting frequency, and FSTOP is the final frequency. At least one independent source must have been specified with an ac value.

### 5.3.2 .DC: DC Transfer Function

The DC analysis of SPICE determines the response of a circuit as a voltage or current source is swept over a given interval. During the analysis, capacitors are assumed to be open and inductors shorted.

Netlist statement:

```
.DC SRCNAM VSTART VSTOP VINCR [SRC2 START2 STOP2 INCR2]
```

Examples:

```
.DC V1 1.00 5.0 0.2  
.DC V2 0 10 .5 V2 0 5 1
```

SRCNAM is the name of an independent voltage or current source. VSTART, VSTOP, and VINCR are the starting, final, and incrementing values respectively. A second source (SRC2) can also be specified. In this case, the first source is

swept over its range for each value of the second source. This is useful for obtaining semiconductor device output characteristics.

### ***5.3.3 .OP: Operating Point Analysis***

The operating point analysis of SPICE determines the state of a circuit with only DC supplies applied. During the analysis, capacitors are assumed to be open and inductors shorted.

Netlist statement:

```
.OP
```

Note that a DC analysis is also automatically performed prior to a transient analysis to determine the transient initial conditions, and prior to an AC small-signal analysis to determine the linearized, small-signal models for nonlinear devices.

Note: To view the results of the .OP analysis, load the circuit's .OUT file with an ASCII editor such as NOTEPAD

### ***5.3.4 .TRAN: Transient Analysis***

The transient analysis of SPICE determines the time response of a circuit. The inputs signals of the circuit can be time dependent functions including piecewise linear, pulse, sinusoidal, exponential and others.

Netlist statement:

```
.TRAN TSTEP TSTOP [TSTART [TMAX]] [UIC]
```

Examples:

```
.TRAN 1NS 200NS  
.TRAN 1NS 400NS 200NS
```

TSTEP is the printing increment for the print command output. For use with the post-processor, TSTEP is the suggested computing increment. TSTOP is the final time, and TSTART is the initial time. If TSTART is omitted, it is assumed to be zero. The transient analysis always begins at time zero. In the interval [zero, TSTART], the circuit is analyzed (to reach a steady state), but no outputs are stored. In the interval [TSTART, TSTOP], the circuit is analyzed and outputs are stored. TMAX is the maximum step size that SPICE uses. By default, the program chooses the smaller of TSTEP or (TSTOP-TSTART)/50.0. TMAX is useful to guarantee a computing interval that is smaller than the printer increment, TSTEP.

UIC (use initial conditions) is an optional keyword that indicates that the user does not want SPICE to solve for the quiescent operating point before beginning the transient analysis. If this keyword is specified, SPICE uses the values specified using IC=... on the various elements as the initial transient condition and proceeds with the analysis. If the IC control line has been specified, then the node voltages on the IC line are used to compute the initial conditions for the devices.

### ***5.3.5 .PZ Pole-Zero Analysis***

Netlist statement:

```
.PZ NODE1 NODE2 NODE3 NODE4 CUR POL
```

```
.PZ NODE1 NODE2 NODE3 NODE4 CUR ZER
.PZ NODE1 NODE2 NODE3 NODE4 CUR PZ
.PZ NODE1 NODE2 NODE3 NODE4 VOL POL
.PZ NODE1 NODE2 NODE3 NODE4 VOL ZER
.PZ NODE1 NODE2 NODE3 NODE4 VOL PZ
```

Examples:

```
.PZ 1 0 3 0 CUR POL
.PZ 2 3 5 0 VOL ZER
.PZ 4 1 4 1 CUR PZ
```

CUR stands for a transfer function of the type (output voltage)/(input current) while VOL stands for a transfer function of the type (output voltage)/(input voltage). POL stands for pole analysis only, ZER for zero analysis only and PZ for both. This feature is provided mainly because if there is a nonconvergence in finding poles or zeros, then, at least the other can be found. Finally, NODE1 and NODE2 are the two input nodes and NODE3 and NODE4 are the two out- put nodes. Thus, there is complete freedom regarding the output and input ports and the type of transfer function.

### 5.3.6 *.TF Transfer Function Analysis*

Netlist statement:

```
.TF OUTVAR INSRC
```

Examples:

```
.TF V(5, 3) VIN
.TF I(VLOAD) VIN
```

The TF line defines the small-signal output and input for the dc small-signal analysis. OUTVAR is the small- signal output variable and INSRC is the small-signal input source. If this line is included, SPICE computes the dc small-signal value of the transfer function (output/input), input resistance, and output resistance. For the first example, SPICE would compute the ratio of V(5, 3) to VIN, the small-signal input resistance at VIN, and the small- signal output resistance measured across nodes 5 and 3.

### 5.3.7 *.NOISE Noise Analysis*

Netlist statement:

```
.NOISE V(OUTPUT <,REF>) SRC ( DEC | LIN | OCT ) PTS FSTART FSTOP <PTS_PER_SUMMARY>
```

Examples:

```
.NOISE V(5) VIN DEC 10 1kHz 100Mhz
.NOISE V(5,3) V1 OCT 8 1.0 1.0e6 1
```

The Noise line does a noise analysis of the circuit. OUTPUT is the node at which the total output noise is desired; if REF is specified, then the noise voltage V(OUTPUT) - V(REF) is calculated. By default, REF is assumed to be ground. SRC is the name of an independent source to which input noise is referred. PTS, FSTART and FSTOP are .AC type parameters that specify the frequency range over which plots are desired. PTS\_PER\_SUMMARY is an optional integer; if specified, the noise contributions of each noise generator is produced every PTS\_PER\_SUMMARY frequency points.

The .NOISE control line produces two plots - one for the Noise Spectral Density curves and one for the total Integrated Noise over the specified frequency range. All noise voltages/currents are in squared units (V /Hz and A /Hz for spectral density, V and A for integrated noise).

## ***5.4 Output (Print Command)***

Netlist statement:

```
.PRINT TYPE CV1 [CV2 ... CV8]
```

Examples:

```
.PRINT TRAN V(4) V(15)  
.PRINT DC V(2) V(18)  
.PRINT AC V(2) VP(2)
```

The output command causes the listing of one to eight circuit variables in the SPICE output (.OUT) file. TYPE is the type of the analysis (DC, AC, or TRAN) for which outputs are desired. Note that the SuperCAD netlister automatically generates this statement based on marked nodes. Marked nodes are those shown on the schematic with numbers and an asterisk suffix (e.g., 2\*, 34\*).

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